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Modified sample and hold circuit for SAR-ADC

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ABSTRACT

Multistep analog to digital converters employs a sample and hold circuit to achieve high linearity with high gain. The sampling circuits further more alleviate the timing and bandwidth limitation of the data converters. This paper explicates the design of a modified sample and hold circuit which utilize the cascode bias. The sampling architecture removes the restrictions on the bandwidth and speed with high linearity. This proposed architecture aides the successive approximation register ADC with optimum performance. The modified sample and hold circuit is designed with a 3.3 V supply in a 0.25μm CMOS process samples at 10 GS/s.

Keywords: High-speed linear integrated circuits, sample and Hold circuit, sampled data circuits

INTRODUCTION

Increasing virtualization, improvement of quality of interfaces are some of the major problems faced in today's world. The interface between the real world and the digital world is exponential complicating every day. A solution for this challenging problem requires to be addressed more efficiently. An analog-to-digital converter (ADC) becomes a critical component for the system that interfaces to the outside world...For any data conversion system, the choice is made on the type of application and the resolution required. The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. Usually the values are stored in binary form electronically; therefore the resolution is expressed in the form of binary digits. Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications with sample rates under 5 mega samples per second (maps). For Successive-approximation-register (SAR) analog-to-digital converter the resolution exists in the range of 8 to 16 bits, and this type of ADCs usually has low power consumption as well as a small form factor. Because of these special features Successive-approximation-register type analog-to-digital converters are suitable for wide variety of applications. The applications are listed as they are used in Control systems, Programmable Logic Controllers, Sensor integration (Robotics), Cell phones, Video devices, Audio devices and in Data Acquisition. A sample and hold circuit is an analog device that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimal period of time. In many cases, the use of a sample and hold can greatly minimize errors due to slightly different delay times in the internal operation of the converter. The sampling pedestal or a hold step, this is an error that occurs each time a sample mode to hold mode .During this change in operation ,there is always a small error in the voltage being held that makes it different from the input voltage at the time of sampling ,this error should be minimized. In well designed sample and holds, this signal feed through can be reduced to its maximum.

Modified sample and hold circuit: The simplest sample and hold that can be realized using a CMOS technology is when Φ_{clk} is high, V' follows V_{in} when Φ_{clk} goes low, V' will ideally stay constant from then on, having a value equal to V_{in} at the instance Φ_{clk} went low. The V' will have a negative going hold step at this time caused by the channel charge of Q1,When Q1 turns off, its channel charge must flow out from under its gate into its junction .since this charge is negative, it will cause the junction voltages to have negative glitches. If one assumes the source impedance at the node V_{in} is very low, then the glitch at this node will be small and have a very short duration however, the negative charge that goes to the node with C_{hid} connected to it will cause a negative voltage change that is long lasting. If clock Φ_{clk} turns off fast, then the channel charge, Q_{CH}, will flow equally into both junctions since the channel becomes pinched off at the both ends While the charge is flowing out to the two junctions .the charge flowing to the junction labeled V' is therefore given by

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox}WLV_{eff-1}}{2} \qquad \text{----------(1)}$$

Where Veff-1 is given by

$$V_{eff-1} = V_{GSi} - V_{tn} = V_{DD} - V_{tn} - V_{in} \qquad \text{----------(2)}$$

Here, V_{in} is the input voltage at the instance Q1 turns off. It should be noted here that this result assumes that the clock signal, Φ_{clk} goes between VDD and the most negative voltage in the circuit. The change in the voltage V' is the found by using the relationship Q=CV, resulting in the equation

$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{ox}WLV_{eff\text{-}1}}{2C_{hld}} = -\frac{C_{ox}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}} \text{----------(3)}$$

That ΔV' is linearity related to Vin which results in a gain error for the overall sample and hold circuit. ΔV'is also linearity related to Vtn ,which is nonlinearity related to the input signal , Vin due to variations in the source substrate voltage this nonlinear relationship with Vin results in distortion for the overall sample and hold circuit.There is also an additional change in V' due to the gate overlap capacitance using a derivation similar to that used to find, we have, (Li et al (2009))

$$\Delta V' \cong -\frac{C_{ox}WL_{ov}(V_{DD} - V_{SS})}{C_{hld}} \text{----------(4)}$$

Where Vss is the most negative voltage in the circuit. This component is usually smaller than that due to the channel charge, and appears simply as an offset since it is signal independent .therefore this error component is not typically important since signal independent offsets can often be removed in most systems, however it may cause noise problems if care is not taken to ensure that the clock signal, Φ_{clk} is relatively noise free.The feedback is included in sample and hold circuit by adding feedback loop in an op amp, when the clock, Φ_{clk} is high, the complete circuit responds similarly to an op amp in a unity gain feedback configuration. When the Φ_{clk} goes low, the input voltage at that time is stored on Chld, similarly to a simple sample and hold by including an op amp in the feedback loop, the input impedance of the sample and hold is greatly increased.

Another advantage of this configuration is that even if the unity gain buffer at the output has an offset voltage, the dc error due to this buffer will be divided by the gain of the input op amp. Thus very simple source followers can be used for the output buffer(Li et al (2009)).A disadvantage of the configuration is that the speed of operation can be seriously degraded due to the necessity of guaranteeing that the loop is stable when it is closed .another source of speed degradation is that when in hold mode, the op amp is open loop, resulting in its output almost certainly saturating at one of the power supply voltages. When the sample and hold next goes back into track mode, it will take some time for the op amp output voltage to slew back to its correct closed loop value.

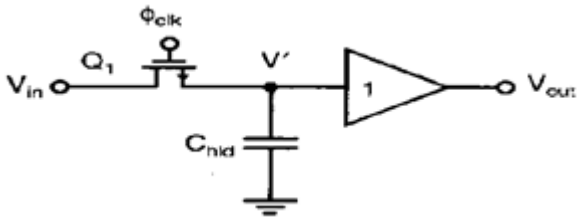

Fig. 1 Open loop sample and hold circuit

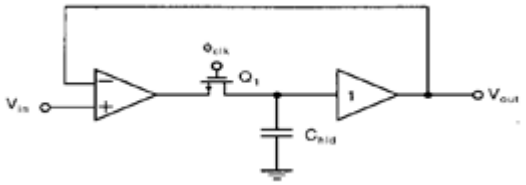

Fig. 2 Closed loop sample and hold circuit

Design and simulation: The sample & hold circuit shown in fig.3 consists of the Input switching network and differential inputs that convert the input voltage difference to differential voltages applied to the positive and negative delay lines .the bias point of the delay cell and the conversion gain are optimized for the Highest possible linearity(Li, 2009).

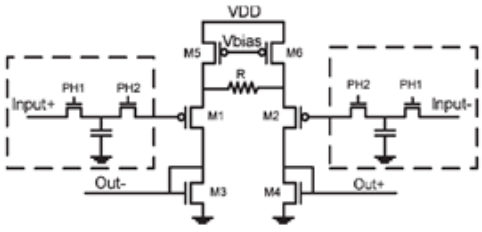

Fig.3.Input sample/hold and Voltage to Current converter

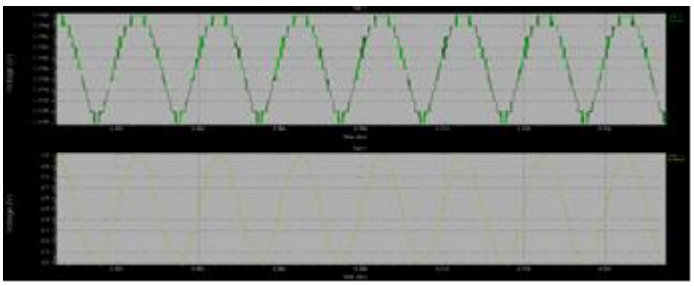

Fig.4.Tanner diagram of sample and hold circuit

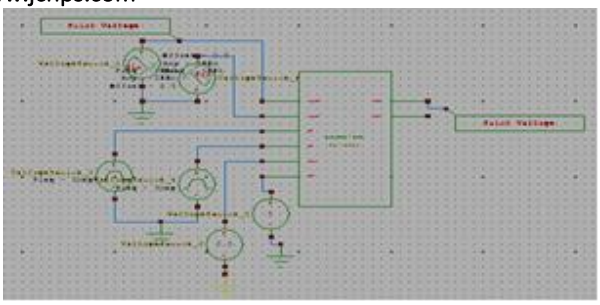

Fig.5.Symbol created of sample and hold circuit using tanner tool

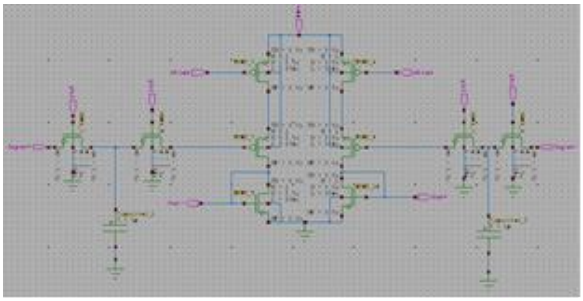

Fig.6.Output of sample and hold

Design specification: The sample and hold circuit is produce to the Total power consumption is 2.7mW from a 3.3 V supply, the input voltage range of the circuit is limited to 0.2 Vppd, Which is much lower than that reported in (Orser Gopi, 2010), due to headroom limitations imposed by the lower supply voltage. Droop rate for this circuitry outperforms previously reported results, with 0.002 *m*V droop for a held value compared to 0.2 *m*V in(Orser Gopi, 2010).The small area, high speed, and low voltage operation of this Circuitry facilitates the design of the multigigahertz Sample and Hold, and by extension ADCs, using standard power supplies in existing CMOS processes.

Table.1.Performance Comparison

	1	2	3	This Work
Process	0.18µm CMOS	0.13µm CMOS	0.13µm CMOS	0.25µm CMOS
Supply Voltage	1.8V and 3.3V	1.8V	1.2V	3.3V
Bandwidth	800MHz	7GHz	1.8GHz	0.1GHz
PERFORMANCE COMPARISION				
Sampling Rate	1.6GS\s	30GS\s	20GS\s	10GS\s
Full Scale input Voltage	0.4Vppd		0.2Vppd	0.2Vppd
Droop rate at sampling speed		0.2mV	0.002mV	0.002mV
Power consumption	183mW	166mW	71mW	2.7mW

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CONCLUSION

A Sample-and-hold architecture suitable for low power, high speed data conversion operation has been presented. The circuit operates at 3.3V, lower than previously reported sample and hold circuit employing the cascade architecture. The architecture has high linearity and bandwidth which make it as ideal sample and hold circuit for data converter with medium resolution like SAR ADC as it trades the disadvantages of SAR ADC, with its advantages. The droop rate at sampling speed is also reduced comparable to the previous architecture. Power consumption is also significantly lower than previously reported sample and hold circuit.

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